REMARKS

Claims 1-29 were examined and rejected. Applicants amend claims 1, 4-6, 13, 21, 24 and 27-28. Applicants assert that no new matter is added therein, as the amendments to the claims to include "an asynchronous communications device test protocol" are supported at least at paragraphs [0012], [0013] and [0015] of the application; to include "asynchronous communications test specification" are supported at least at paragraphs [0015], [0027], [0031]-[0032], [0037] and [0039] of the application; to include "skip-order-sets included in the test data received" are supported at least at paragraphs [0038] and [0039] of the application; to include "a processor coupled to a memory; the memory storing data that when executed by the processor causes the processor to implement a test protocol including:" are supported at least at paragraphs [0013] and [0037] of the application; and to require "the first and second chips are different types of digital communication chips" or "during an asynchronous communications test of actual, not simulated, communications data" are supported at least at paragraphs [0056] and [0057] of the application, respectively. Hence, Applicants respectfully request reconsideration of the pending claims.

I. Claims Rejected Under 35 U.S.C. § 112

Claims 1-29 are rejected under 35 U.S.C. § 112, second paragraph, because it is not clear whether the claims describe actual hardware devices and/or methods of using actual hardware devices.

Applicants have amended independent apparatus claim 13 and independent system claims 21 and 27 to include a processor and a memory storing data that when executed by the processor causes the processor to implement an asynchronous communications device test protocol. Hence, Applicants respectfully request the Patent Office withdraw the rejection above for claims 13-29.

With respect to method claims 1-12, Applicants respectfully disagree and submits that, upon reading the specification and the claims, a practitioner in the art would find the method claims definite, such as by representing methods of using simulated devices and actual hardware devices, as described in the application.

Similarly, with respect to article of manufacture claims 24-26, upon reading the specification, a practitioner in the art would find such claims clear. Hence, Applicants respectfully request the Patent Office withdraw all of the rejections above.

III. Claims Rejected Under 35 U.S.C. § 103

The Patent Office rejects claims 1, 2, 5, 6 and 21 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 7,007,212 to Komatsu et al. (Komatsu) in view of U.S. Patent No. 6,023,777 to Knaack (Knaack). The Patent Office rejects claims 4, 10, 13 and 24 under 35 U.S.C. § 103(a) as being unpatentable over Komatsu and Knaack as applied to claim 1 above, and further in view of U.S. Patent No. 6,347,380 to Chang et al. (Chang). The Patent Office rejects claim 27 under 35 U.S.C. § 103(a) as being unpatentable over Komatsu and Knaack as applied to claim 1 above, and further in view of U.S. Patent No. 6,476,628 to LeColst (LeColst). To be obvious, every limitation of a claim must be taught by at least one properly combined reference.

Applicants respectfully disagree with respect to independent claim 1 for at least the reason that the cited references do not teach shifting the input clock frequency to an output clock frequency based on an asynchronous communications device test protocol, as required by amended claim 1.

Komatsu teaches testing high-speed serial data interfaces such as DVI and IEEE1394 for high-speed transmission (see Abstract and col. 1, lines 16-25). However, Komatsu does not teach or enable the above-noted limitations of claim 1.

Knaack teaches testing FIFO buffers, typically employing a variety of status flags (see Abstract and col. 1, lines 12-31). Knaack also teaches changing a difference between clocks, such that a write clock may be ahead of a read clock by a different phase or period of time (see col. 4, lines 27-57). However, Knaack does not teach or enable the above-noted limitations of claim 1.

Chang teaches a phase locked loop to avoid memory overflow and underrun by monitoring a difference between write and read pointers of audio data being written into and read from FIFO 40 (see Abstract, Figure 6, and col. 8, lines 27-66). However, Chang does not teach or enable the above-noted limitations of claim 1.

LeColst teaches a semiconductor parallel tester for simultaneously testing a plurality of DUTs secured to a handling apparatus (see Abstract, Figure 1 and col. 1, lines 22-37). However, LeColst does not teach or enable the above-noted limitations of claim 1.

In addition to being dependent upon allowable claim 1, Applicants disagree with the rejection above of claim 4 for at least the reason that none of the references teach

setting the output clock frequency to greater than the input clock frequency while the test data retained is greater than an asynchronous communications test specification upper watermark; and setting the output clock frequency to less than the input clock frequency while the test data retained is less than an asynchronous communications test specification lower watermark, as required by amended claim 4. Teachings of the references are noted above with respect to claim 1. Consequently, the Patent Office has not identified and Applicants are unable to find any teaching in the references of setting an output clock frequency related to an upper watermark or a lower watermark of an asynchronous communications test specification, as required by claim 4.

In addition to being dependent upon base claim 1, Applicants disagree with the rejection of dependent claim 5 for at least the reason that none of the references teach or enable increasing an output clock frequency to a selected maximum output data frequency based on an asynchronous communications test device protocol and decreasing the output clock to a selected minimum frequency based on an asynchronous communications test device protocol, as required by amended claim 5. The teachings of the references are noted above with respect to claim 1. However, the Patent Office has not identified and Applicants are unable to find any teaching or enablement in the references of the above-noted limitations of dependent claim 5.

In addition to being dependent upon base claim 1, Applicants disagree with the rejection of dependent claim 6 for at least the reason that the references do not teach or enable changing the output clock frequency during the period of time depending on at least one of skip-order-sets included in the test data received, and a duration between marker types of data packets included in the test data received, as required by amended claim 6. Teachings of the references are noted above with respect to claim 1. However, the Patent Office has not identified and Applicants are unable to find any teaching or enablement in the references of the above-noted limitations of amended claim 6.

Applicants disagree with the rejection above of independent claim 13 for at least the reason that the references do not teach or enable data that when executed by a processor causes the processor to implement an asynchronous communications test device protocol including a lower watermark of the maximum data storage capacity based on an asynchronous communications test device protocol, and an upper watermark of the maximum data storage capacity based on an asynchronous communications test device protocol; and a frequency modifier to shift the input clock

frequency to the output clock frequencies based on an asynchronous communications test device protocol, as required by amended claim 13. Arguments analogous to the one above for claims 1 and 4 apply here as well.

Applicants disagree with the rejection above of independent claim 21 for at least the reason that the cited references do not teach or enable data that when executed by the processor causes the processor to implement an asynchronous communications device test protocol including a digital signal processor that supports asynchronous communications across a link; and a frequency modifier to shift the test frequency to an output clock frequency and to vary the output clock frequency over a period of time based on an asynchronous communications device test protocol, as required by amended claim 21. Argument analogous to the ones above for claim 1 apply here as well.

Applicants disagree with the rejection above of claim 24 for at least the reason that the references do not teach or enable data which when accessed by a processor implements an asynchronous communications device test protocol having a lower watermark based on an asynchronous communications device test protocol and an upper watermark based on an asynchronous communications device test protocol, as required by claim 24. Arguments analogous to the ones above for claims 1 and 4 apply here as well.

Applicants disagree with the rejection above of claim 27 for at least the reason that the references do not teach or enable data that when executed by a processor causes the processor to implement an asynchronous communications device test protocol including a first chip and a second chip, wherein the first and second chips are different types of digital communication chips, as required by amended claim 27.

Descriptions of the teachings of the references are provided above with respect to claim 1. However, none of the references teaches the above-noted limitations of claim 27. Specifically, LeColst teaches simultaneously testing groups of DUTs in parallel (see Abstract, Figure 6 and col. 1, lines 23-37). However, the Patent Office has not identified and Applicants are unable to find any description in LeColst that the DUTs are different types of digital communication chips, as required by claim 27.

Any dependent claims not mentioned above are submitted as being patentable for at least the reasons provided in support of their base claims, as well as any additional limitations of those dependent claims.

Hence, Applicants respectfully request that all of the rejections above be withdrawn.

IV. Claims Not Rejected Under 35 U.S.C. § 103

Applicants note that claims 3, 7-9, 11-12, 14-20, 22-23, 25-26 and 28-29 were not rejected under an anticipation or obviousness-type rejection.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Angelo J. Gaz, Reg. No. 45,907

1279 Oakmead Parkway
Sunnyvale, California 94085-4040
Telephone (310) 207-3800
Facsimile (408) 720-8383

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below to the United States Patent and Trademark Office.

Suzanne Johnston — 6/20/08 Date